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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,122	05/08/2001	Martin Czech	Micronas.6158	4157

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,122	CZECH ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *9-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election of claims 1-8 and 13-15 drawn towards a device, in a Paper filed 11/3/03 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3. Claim 1 is objected to because of the following informalities: line 9 should read "pulse to one **of** the first". Appropriate correction is required.

4. Claim 5 is objected to because of the following informalities: line 2 should read "second region" and "first region" as only one of each region is claimed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 line 7 recites "a doped second conduction type". This limitation is indefinite as one cannot ascertain what is doped the second conduction type or where the doped second conduction type is located. Thus, one cannot ascertain how or where the doped second conduction type relates to the structure of the claim. Also, claim 1 line 7 recites "a gate electrode ... corresponding to the width (W) or the length of the gate electrode." This limitation is indefinite as one cannot ascertain what structurally limitation is necessitated by this language or what structure is being claimed.

Claim 2-8 are similarly rejected as they contain the same limitations of independent claim 1 from which they depend.

7. Insofar as definite, the claims are rejected over prior art as follows. For the sake of the following rejections, claim 1 is being interpreted such that second region is doped a second conduction type and that the gate electrode is formed between the first and second region and has a width (W) or length.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Voldman et al. (U. S. Patent No. 6,015,993).

Voldman et al. disclose an ESD protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential and a second potential bus with a second supply potential, the electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region 142 doped with a first conduction type P and a second region 144 spaced apart from the first region 142, the second region doped a second conduction type N (figure 5);

wherein the electrostatic discharge protective structure is located between the first 232 and second potential busses 234 and drains off an overvoltage pulse to one of the first and second potential busses (figure 12A); and

wherein the laterally formed electrostatic discharge diode includes a gate electrode 136,140 located between the first region 142 and the second region 144 corresponding to the width or the length of the gate electrode (the gate has a lateral length corresponding to the gate electrode) (figure 5).

With regard to claim 2, the protective structure includes a semiconductor body 122 having a surface in which the first and second regions are embedded (figure 5),

wherein the first region is connected via a first electrode to the first potential bus and the second region is connected via a second electrode to the second potential bus (figure 12A). Though the first and second electrode are not explicitly shown, they are nonetheless implicitly disclosed as figure 12A shows the first and second regions (anode and cathode) connected to the busses and one would necessarily have electrodes to provide such connection.

With regard to claim 3, the semiconductor body 122 includes charge carriers of the second conduction type N and the gate electrode and second electrode are connected to the second potential bus (figure 12A, col. 5 line 66 through col. 6 line 13).

With regard to claim 4, the semiconductor body is substrate 124 which includes charge carriers of the first conduction type, and at least one well 122 of the second conduction type is embedded in the semiconductor body 124, the first and second regions 142,144 are embedded in the well 122 (figure 5).

With regard to claim 6, the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit (col. 2 lines 12-13, the ESD protection is for a MOSFET circuit).

With regard to claim 7, Voldman et al. further disclose a gate dielectric 130 that spaces the semiconductor body at a distance from the gate electrode (figure 5).

With regard to claim 8, the gate dielectric contains silicon dioxide and the gate electrode contains polysilicon.

10. Claims 1-3, 6-8 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun et al. (U.S. Patent No. 6,344,385 B1).

Jun et al. disclose an ESD protective structure that protects an integrated semiconductor circuit connected between a first potential bus with a first supply potential and a second potential bus with a second supply potential, the electrostatic discharge protective structure comprising:

a laterally formed electrostatic discharge diode having a first region 13 doped with a first conduction type N and a second region 36 spaced apart from the first region 13, the second region doped a second conduction type P (figure 3a);

wherein the electrostatic discharge protective structure is located between the first 34 and second potential busses (ground) and drains off an overvoltage pulse to one of the first and second potential busses (figure 3a); and

wherein the laterally formed electrostatic discharge diode includes a gate electrode 35 located between the first region 13 and the second region 36 corresponding to the width or the length of the gate electrode (the gate has a lateral length corresponding to the gate electrode) (figure 3a).

With regard to claim 2, the protective structure includes a semiconductor body 11 having a surface in which the first and second regions are embedded (figure 3a), wherein the first region is connected via a first electrode to the first potential bus and the second region is connected via a second electrode to the second potential bus (figure 3a).

With regard to claim 3, the semiconductor body 11 includes charge carriers of the second conduction type P and the gate electrode and second electrode are connected to the second potential bus (figure 3a).

With regard to claim 6, the integrated semiconductor circuit is configured and arranged as an MOS or CMOS circuit (figure 3a, the circuit protects the MOS transistor form from source and drain 31 and 32 and gate 33).

With regard to claim 7, Jun et al. further disclose a gate dielectric that spaces the semiconductor body at a distance from the gate electrode (figure 3a).

With regard to claim 8, the gate dielectric contains silicon dioxide and the gate electrode contains polysilicon. The gate 35 is formed the same as the gate 33 of the MOS transistor, and thus discloses the same polysilicon gate and silicon dioxide gate dielectric (col. 3 line 12-35).

With regard to claim 13, Jun et al. disclose an integrated circuit with electrostatic discharge protection comprising:

a circuit (MOS transistor formed by 31,32,33) to be protected (figure 3a);

an electronic discharge device 28 that is disposed electrically parallel to the circuit to be protected between first 34 and second (ground) voltage busses, wherein the electrostatic discharge device includes a laterally shaped electrostatic discharge diode having:

a first region 13 doped with a first conduction type material P within a substrate 11 (figure 3a);

a second region 36 doped with a second conduction type material P within the substrate (figure 3a); and

a gate electrode 35 having a width W and located between the first 13 and second 36 regions such that the first and second regions are separated by the width W (figure 3a).

With regard to claim 14, Jun et al. further disclose a gate oxide disposed on the substrate between the first and second conduction regions and underlying the gate electrode (figure 3a, the gate is disclosed as MOS gate, thus containing an oxide between the gate and the substrate).

With regard to claim 15, Jun et al. do not explicitly disclose an first electrode on the substrate overlying the first region or a second electrode overlying the substrate in the second region. However, Jun et al. do disclose the first region being connected to the first voltage bus and the second region being connected to the second bus. In showing the electrical connection from the substrate to the busses, Jun et al. is implicitly disclosing electrodes to form the connections. One would recognize that electrodes would inherently be formed to provide the electrical connection.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Voldman et al. (U.S. Patent No. 6015993) as applied to claims 1-4 and 6-8 above, and further in view of Williams (U.S. Patent No. 6,060,752).

Voldman et al. teach all the limitations of claim 4, from which claim 5 depends. However, Voldman et al. do not teach the second region laterally enclosing the first region.

Williams teach an electrostatic discharge device including diodes. Williams teach in figure 11A-G various configurations of the first (P) and second (N) regions where the second region laterally encloses the first region.

Voldman et al. and Williams are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the second region to laterally enclose the first region. The motivation for doing so is to provide improved carrier confinement. Therefore, it would have been obvious to combine Voldman et al. with Williams to obtain the invention of claim 5.

Conclusion

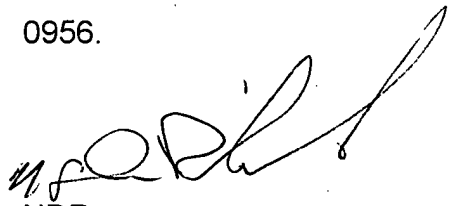
13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kawazoe et al. (U.S. Patent No. 6524893 B2), Ker et al. (U.S. Patent No. 5182220), Ravanelli et al. (U.S. Patent No. 5959332), Chen et al. (U.S. Patent No.5808342), Yamaguchi et al. (U.S. Patent No.6118154), Takao (U.S. Patent

No. 6215138 B1), Yoshida et al. (U.S. Patent No. 6229180 B1), Yamaguchi et al. (U.S. Patent No. 6274908 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



NDR

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